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IN THE CLAIMS:

1. (currently amended) A current mode transfer logic transmission line driver system comprising:

a transmission line, defining at least a first and a second signal carrying conductor, the transmission line defining a characteristic impedance,

means for selectively driving unequal logic signal currents through the first and the second signal carrying conductors, respectively,

a terminating resistor connected between the distal ends of the first and the second signal carrying conductors,

means for receiving the logic signal currents at the distal end of each transmission line, wherein the received currents are unequal to each other, and

means for sensing and amplifying the unequal currents.

2. (previously presented) The current mode transfer logic transmission line driver system of claim 1 wherein the means for selectively driving unequal currents through the two transmission lines, comprises:

a first current source selectably connected to the first signal carrying conductor, and

a second current source selectably connected to the second signal carrying conductor of the first transmission line, the first and the second current sources of unequal magnitudes.

3. (previously presented) The current mode transfer logic transmission line driver system of claim 1 wherein the means for receiving currents at the distal end of each transmission line comprises:

a first current receiving circuit connected between the distal end of the first transmission line and at least one return path conductor, and

a second current receiving circuit connected between the distal end of the second transmission line and at least one return path conductor.

4. (currently amended) The current mode transfer logic transmission line driver system of claim ~~1~~ 3 wherein the first and the second current receiving circuits comprises diode connected MOS transistors.

5. (previously presented) The current mode transfer logic transmission line driver system of claim 4 further comprising means for biasing each diode connected MOS transistor so that it presents a low impedance at the distal ends of the transmission lines, but wherein that low impedance is substantially higher than the line's characteristic impedance.

6. (currently amended) The current mode transfer logic line driver system of claim 1 wherein the means for sensing the unequal currents comprises means for comparing the currents in ~~the~~ a first receiving circuit to the current in ~~the~~ a second receiving circuit.

7. (previously presented) The current mode transfer logic line driver system of claim 6 wherein the means for comparing the currents in the first receiving circuit to the current in the second receiving circuit comprises:

a differential current amplifying circuit that amplifies the difference in the currents in the first and the second receiving circuits.

8. (previously presented) The current mode transfer logic line driver system of claim 6 wherein the differential current amplifying circuit comprises:

a first amplifying current mirroring circuit providing an first output current,

a second amplifying current mirroring circuit providing a second output current, and

a current to voltage conversion circuit, arranged to receive the first and the second output currents and provides a voltage output that is proportional to the difference between the outputs of the first and the second amplifying current mirroring circuits.

9. (previously presented) The current mode transfer logic transmission line driver system of claim 1 wherein the transmission line comprises:

a first transmission line defining the first signal carrying conductor and a characteristic impedance with respect to at least one return path conductor,

a second transmission line defining the second signal carrying conductor and a characteristic impedance with respect to at least one return path conductor,

wherein the at least one return path conductor is connected to ground.

10. (currently amended) A method for transferring current mode logic signals over transmission lines comprising the steps of::

defining a transmission line with at least a first and a second signal carrying conductor,

defining a characteristic impedance with respect to the at least first and second signal carrying conductors,

selectively driving unequal logic signalcurrents through the two signal carrying conductors,

providing a terminating resistor between the distal ends of the at least first and the second signal carrying conductors,

receiving the logic signal currents from the distal end of the transmission line, wherein the received currents are unequal to each other, and

sensing and amplifying the unequal currents.

11. (previously presented) The method for transferring current mode logic signals of claim 9 wherein the selectively driving unequal currents through the two signal carrying conductors, comprises the steps of:

selectably connecting a first current source to the first signal carrying conductor, and

selectively connecting a second current source to the second signal carrying conductor, wherein the first and the second current sources are of unequal magnitudes.

12. (previously presented) The method for transferring current mode logic signals of claim 10 wherein the receiving currents from the distal end of the transmission line comprises the steps of:

receiving a first current from the distal end of the first signal carrying conductor, and

receiving a second current from the distal end of the second signal carrying conductor.

13. (previously presented) The method for transferring current mode logic signals of claim 12 wherein the first and the second currents are received by diode connected MOS transistors.

14. (previously presented) The method for transferring current mode logic signals of claim 13 further comprising the steps of biasing each diode connected MOS transistor so that it presents a low impedance at the distal ends of the transmission lines, but wherein that low impedance is substantially higher than the line's characteristic impedance.

15. (currently amended) The method for transferring current mode logic signals of claim 10 wherein the step of sensing the unequal currents comprises the step of comparing the current in ~~the~~ a first receiving circuit to the current in ~~the~~ a second receiving circuit.

16. (previously presented) The method for transferring current mode logic signals of claim 15 wherein the step of comparing the currents in the first receiving circuit to the

current in the second receiving circuit comprises the step of amplifying the difference in the currents in the first and the second receiving circuits.

17. (previously presented) The method for transferring current mode logic signals of claim 15 wherein the step of amplifying the difference comprises the steps of:

first mirroring and amplifying the current in the first receiving circuit and providing an first output current,

second mirroring and amplifying the current in the first receiving circuit and providing a second output current,

receiving the first and the second output currents, and

provides a voltage output that is proportional to the difference between the received first and the second output currents.

18. (previously presented) The method for transferring current mode logic signals of claim 10 wherein the step of defining a transmission line comprises the steps of:

defining a first transmission line having the first signal carrying conductor and a characteristic impedance with respect to at least one return path conductor, and

defining a second transmission line having the second signal carrying conductor and a characteristic impedance with respect to at least one return path conductor, wherein the at least one return path conductor is connected to ground.